CS 315-01 Processor Design Components

Project 05 → incremental development

C Coding
Data Representation
Memory
RISC-V Assembly
RISC-V Machine Code
RISC-V Emulator
Cache Design
Digital Design

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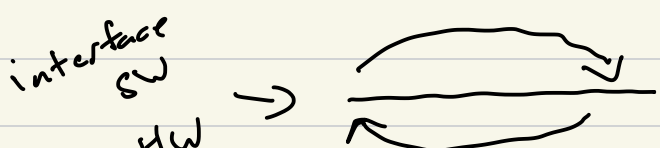
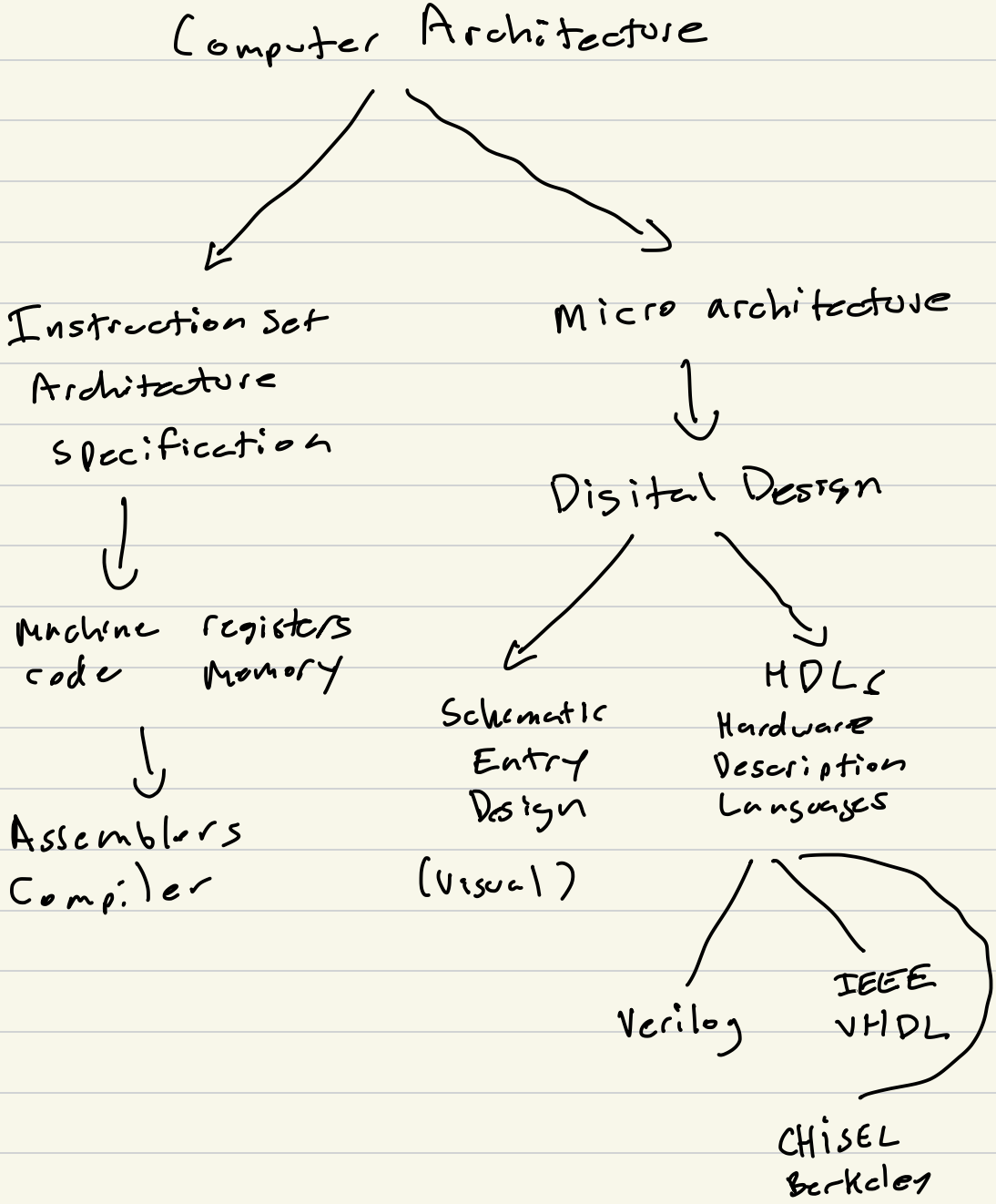
Processor Design

Instruction Set Architecture (ISA)



micro architecture
digital logic implementation


Computer Architecture
Instruction Set Architecture Specification
Micro architecture
Digital Design
Machine code
registers
Memory
Assemblers
Compiler
Schematic Entry Design
(Visual)
HDLs
Hardware Description Languages
Verilog
IEEE VHDL
CHISEL
Berkeley

Processor Design

Moore's Law

The number of transistors doubles every 1.5 years

↑

increase size
increase density

Two

Micro architectures

single-cycle processor
[multi-cycle]
pipelined processor

} this class

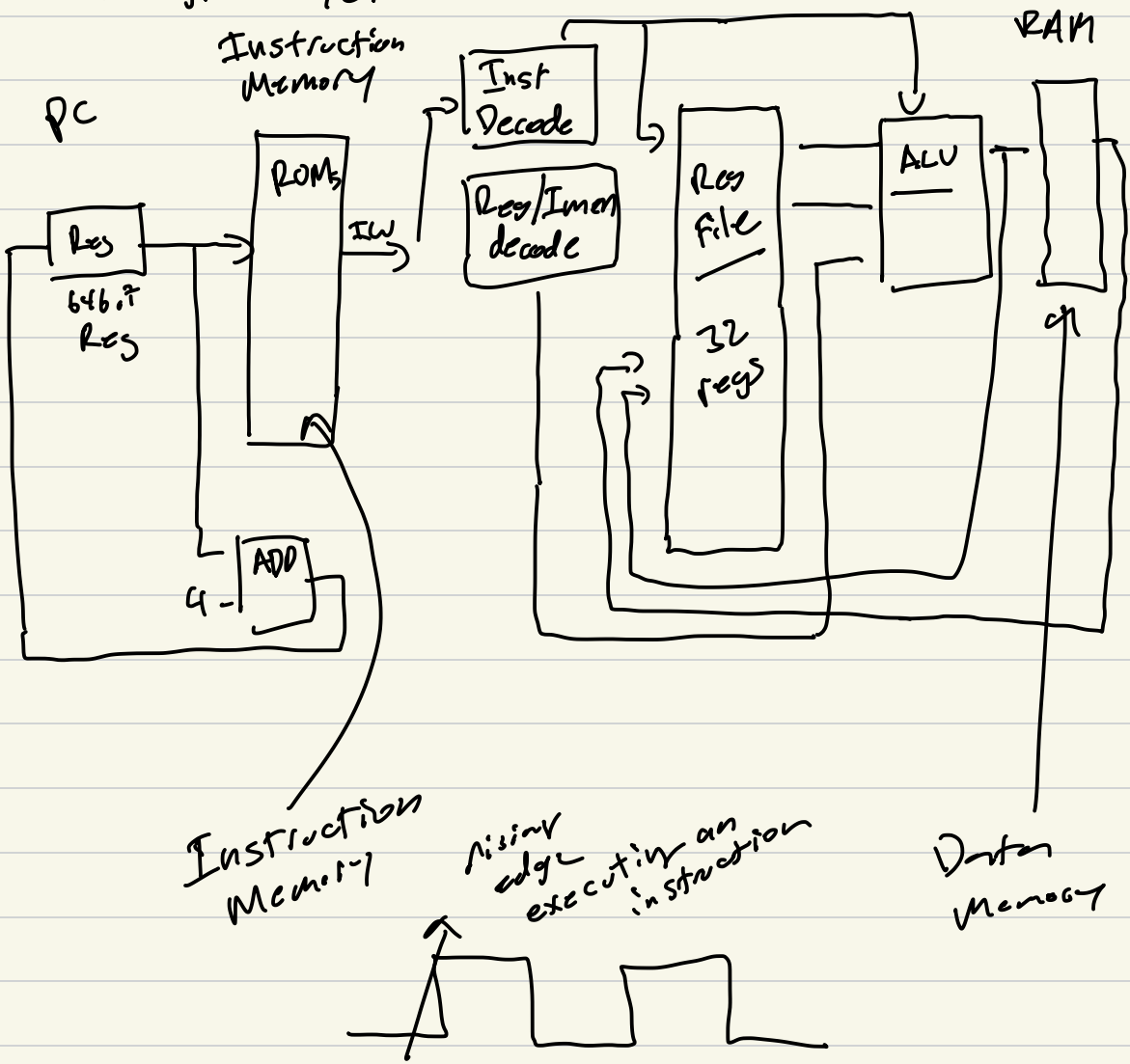
super scalar
Out of order execution
Speculative execution

Lab 05 → Lab 06 → Project 06

↑

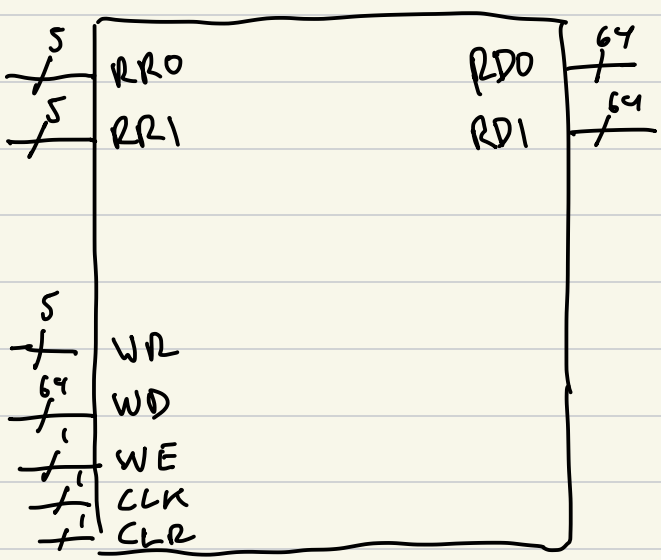
Single-cycle RISC-V ←

Single Cycle Processor



Register File

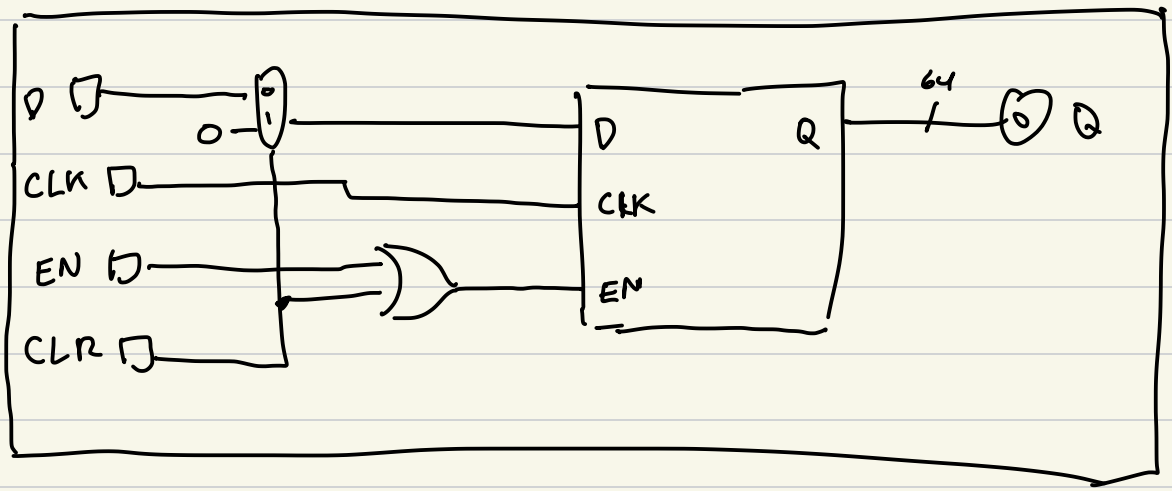
- 32 64-bit Registers $x0, x1, \ldots, x31$
- Read up to two register values on a single clock cycle.
- Write to one register on a single clock cycle
- X0 (zero) will always be zero (no updates)



RR read register #
RD read data

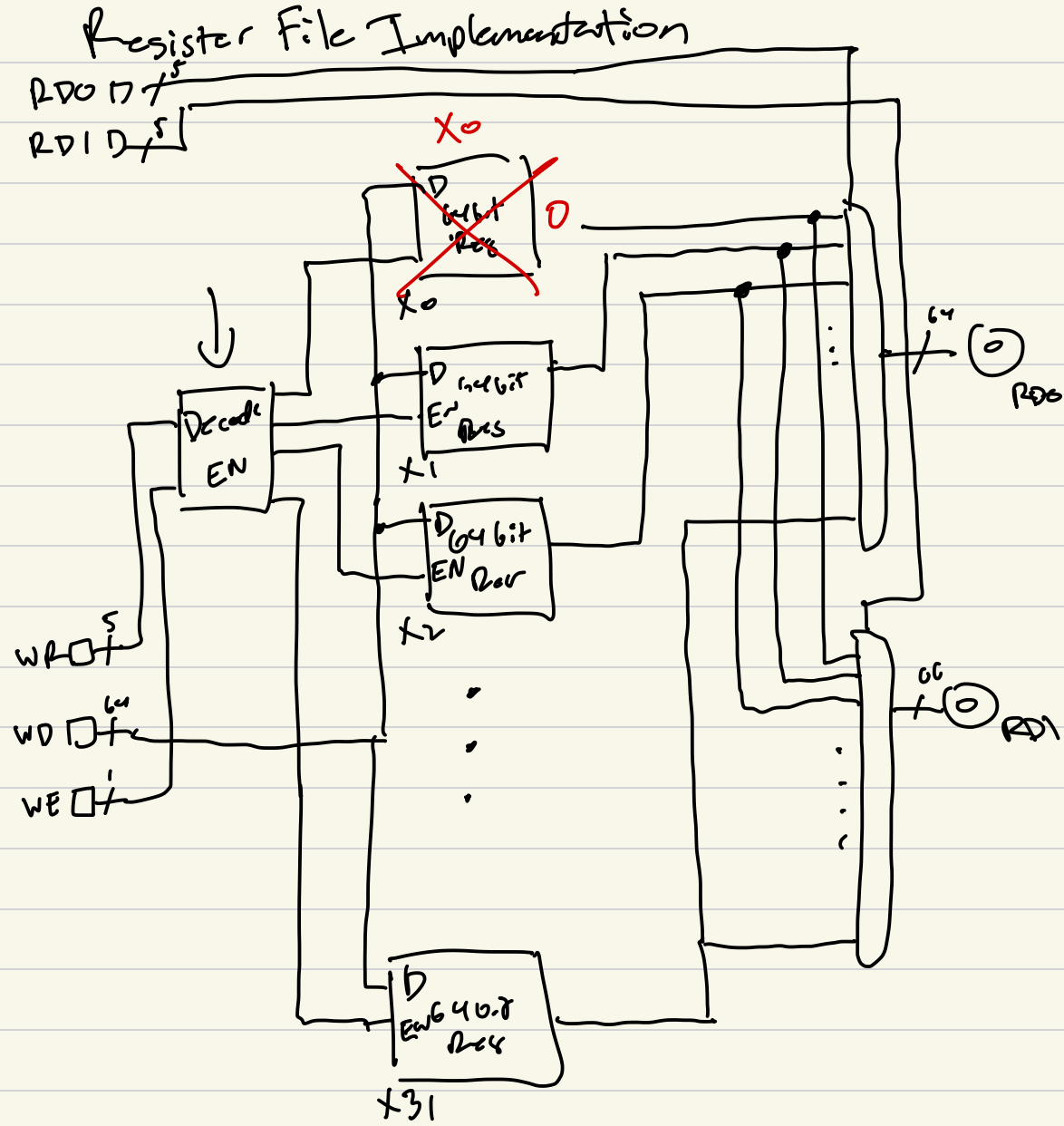
WR write register
WD write data
WE write enable

Adding CLR to Digital Register



64 bit Register with CLR

Synchronous


Register File Implementation
RD0
5
RD1
5
X0
D
64 bit Reg
Q
X0
D
64 bit Reg
EN
Decode
EN
X1
D
64 bit Reg
EN
X2
64
RD0
WR
5
WD
64
WE
1
D
64 bit Reg
EN
X31